



Name:..... 3rd / 4th year B.N : Score :

1. (10 points) Identify the choice that best completes the statement or answers the question.
 - (1) If $ES = D321H$, then the range of physical addresses for the extra segment is:
A. $00000H - 0D321H$ C. **$D3210H - E320FH$**
B. $D3210H - D321FH$ D. $0D321H - 1D320H$
 - (2) What is the largest signed integer that may be stored in 32 bits?
A. $2^{32} - 1$ B. $2^{31} - 1$ C. 2^{32} D. 2^{31}
 - (3) The _____ allows the program to single step (execute one instruction at a time).
A. Carry Flag B. Direction Flag C. **Trap Flag** D. Parity Flag
 - (4) Why you use Memory Segmentation in 8086 Microprocessor?
A. allow the processor to access 64kb of memory
B. **allow the processor to access more than 64kb of memory**
C. None of the above
 - (5) What will be the contents of register AL after the following has been executed
MOV BL, 8C
MOV AL, 7E
ADD AL, BL
A. **0A and carry flag is set** C. 0A and carry flag is reset
B. 6A and carry flag is set D. 6A and carry flag is reset
 - (6) Data transfer instructions will.
A. Affect flag register C. Use RSI and RDI registers
B. **Not affect flag register** D. Non of the above
 - (7) Which mode does Windows use?
A. Real mode B. **Protected mode** C. Flat mode D. None of the above
 - (8) If $CS = 7FA2H$, $SS = 0801H$, $SI = 0100H$ and $IP = 438EH$ the address of the next instruction is:
A. **83DAEH** B. 438EH C. 83DA0H D. 438FH
 - (9) In protected mode memory addressing segment registers used as
A. A selector to global descriptor table
B. A selector to local descriptor table
C. A segment register for real mode segments
D. **A selector to either local or global descriptor table**
 - (10) What type of circuit is used to provides signal protection and amplification
A. Decoder B. Latch C. **Buffer** D. Register
 - (11) The basic parts of an instruction, in order from left to right, are:
A. comment, label, mnemonic, operand(s) C. label, mnemonic, comment
B. **label, mnemonic, operand(s), comment** D. mnemonic, operand(s), comment

- (12) A machine cycle refers to
- | | |
|---|------------------|
| A. fetching an instruction | struction |
| B. executing an instruction | D. clock speed |
| C. fetching, decoding and executing an in- | |
- (13) Which flag does the 80x86 use to check for unsigned arithmetic overflow?
- | | | | |
|-------|-------|--------------|----------------------|
| A. OF | B. SF | C. CF | D. None of the above |
|-------|-------|--------------|----------------------|
- (14) SP is associated withBy default
- | | | | |
|-------|-------|--------------|-------|
| A. ES | B. DS | C. SS | D. CS |
|-------|-------|--------------|-------|
- (15) What is the memory address of the next instruction if CS = 3456H and IP = ABCDH
- | | | | |
|----------|----------|------------------|-----------|
| A. E023H | B. ABCDH | C. 3F12DH | D. AF126H |
|----------|----------|------------------|-----------|
- (16) Which register are used as an offset address for the string instruction destination in the microprocessor?
- | | | | |
|-------|-------|--------------|-------|
| A. SI | B. DX | C. DI | D. BX |
|-------|-------|--------------|-------|
- (17) What is the purpose of the segment register in protected mode memory addressing?
- | | |
|---|---|
| A. selects the descriptor from a descriptor table | C. chooses either the global or local table |
| B. sets privilege level | D. All of the above |
- (18) The program-invisible registers are
- | | |
|---------------------------------------|-------------------------------|
| A. The segment registers cache | C. paging registers |
| B. segment registers | D. Operating system registers |
- (19) The computer architecture aimed to reducing the time of execution of instructions is
- | | | | |
|---------|----------------|---------|--------|
| A. CISC | B. RISC | C. 8086 | D. ISA |
|---------|----------------|---------|--------|
- (20) Stack memory is maintained by two registers
- | | | | |
|----------|-----------------|----------|----------------------|
| A. BP,BI | B. SS,SP | C. CS,SP | D. None of the above |
|----------|-----------------|----------|----------------------|
2. (3 points) List with examples 5 different addressing mode.

Solution:

3. (3 points) Briefly describe the purpose of each T state timing including the wait state in the 8086 processor read bus cycle.

Solution:

4. (3 points) Calculate the memory access time of a 10 MHz processor. Assume address valid delay (T_{CLAV}) is 90 ns, data setup time (T_{DVCL}) is 40 ns,

Solution:

5. (3 points) What is the operation of 8086 pin Connections ALE, INTR and NMI.

Solution:

6. (3 points) What is the difference of processor operating modes (real , protected and flat mode).

Solution:

7. (3 points) [Bonus Question] Why processors implement Memory Paging as a memory management technique ? What is the purpose of Write Through (WT) and Dirty bits in page registers.

Solution:

*With My Best Wishes
Dr. Ahmed Bayoumi*